IN THE CLAIMS:

1. (Currently amended) A high voltage isolation barrier structure, comprising:

a circuit board comprising a substrate, the substrate comprising a first side and a second side, the first side having a first circuitry and a second circuitry;

a capacitive structure comprising:

a **plurality of** first ~~electrode~~ **electrodes** disposed on the first side of the substrate;

a **plurality of** second ~~electrode~~ **electrodes** disposed on the second side of the substrate; and

a **plurality of** conductive **[[via]]** **vias** through the substrate; and

wherein the substrate intermediate the **plurality of** first and second electrodes functions as a dielectric material within the capacitive structure;

the **plurality of** first ~~electrode~~ **electrodes** is electrically coupled to said first circuitry; and

the **plurality of** conductive **[[via]]** **vias** electrically couples the **plurality of** second ~~electrode~~ **electrodes** to the second circuitry, **wherein the plurality of first and second electrodes are shaped and located so as to utilize otherwise unused portions of the surfaces of the substrate while providing high voltage isolation between the first circuitry and the second circuitry**.

Claim 2 (cancelled).

3. (Original) The high voltage isolation barrier structure of claim 1, wherein the circuit board is contained within a data access arrangement.

4. (Currently amended) The high voltage isolation barrier structure of claim 1, wherein the circuit board is ~~contained within a computer system~~ **a fiberglass circuit board.**

5. (Original) The high voltage isolation barrier structure of claim 4, wherein the computer system further comprises a modem; and

the capacitive structure is contained within the modem.

6. (Original) The high voltage isolation barrier structure of claim 1, wherein the circuit board comprises radio frequency circuitry.

7. (Original) The circuit board capacitor structure of claim 1, wherein the circuit board comprises a multi-layer circuit board having a plurality of substrates.

8. (Currently amended) A data access arrangement, comprising:

a circuit board having a substrate with a first side and a second side;

a conductive via through the substrate;

a **high voltage isolation** capacitor having a first electrode formed on the first side of the substrate and a second electrode formed on the second side of the substrate;

system side circuitry coupled to the first electrode and located on the first side; and

line side circuitry coupled to the second electrode and located on the first side;

wherein the conductive via couples the second electrode to the line side circuitry.

9. (Original)The data access arrangement of claim 8, the system side circuitry is configurable to communicate with host system circuitry, and the line side is configurable to communicate over a telephone network.

Claim 10 (cancelled).

11. (Original)The data access arrangement of claim 8, wherein the first and second electrodes are substantially overlapping.

12. (Original)The data access arrangement of claim 8, wherein at least two portions selected from a portion of the system side circuitry and a portion of the line side circuitry are formed on opposite sides of the substrate.

13. (Original)The data access arrangement of claim 8, the first and second electrodes being formed of copper.

14. (Original)The data access arrangement of claim 8, wherein data and control information are communicated between the system side circuitry and the line side circuitry in a serialized digital format via the capacitor.

15. (Original)The data access arrangement of claim 8, further comprising:

at least one additional capacitor having a first electrode formed on the first side of the substrate and a second electrode formed on the second side of the substrate, the at least one additional capacitor coupled between the system side circuitry and the line side circuitry.

16. (Original)The data access arrangement of claim 8, wherein the circuit board comprises a multi-layer circuit board having a plurality of substrates.

17. (Original)The data access arrangement of claim 8, the first electrode being formed on a plurality of substrates.

18. (Original)The data access arrangement of claim 8, wherein the first and second electrodes are printed on the substrate by a screening process.

19. (Previously presented) A method of manufacturing a communications device, comprising:

providing a circuit board having at least one substrate with a first side and a second side;

forming a first electrode on the first side of the substrate;

forming a second electrode on the second side of the substrate, wherein the substrate intermediate the first and second electrodes functions as a dielectric material such that a capacitive structure is formed;

forming a conductive via through the substrate;

electrically coupling first communication circuitry to the first electrode, the first communication circuitry being located on the first side; and

electrically coupling second communication circuitry to the second electrode by the conductive via, the second communication circuitry being located on the first side.

20. (Original) The method of claim 19, wherein the first and second communication circuitry and capacitive structure form at least a portion of a data access arrangement.

21. (Original)The method of claim 20, the capacitive structure providing high voltage isolation between the first communication circuitry and the second communication circuitry.

22. (Original) The method of claim 19, wherein the first and second electrodes are substantially overlapping.

Claim 23 (cancelled).

24. (Original) The method of claim 23, the step of forming a first electrode further comprising forming the first electrode on the sides of more than one substrate.

25. (Original) The method of claim 19, further comprising:

providing the first communication circuitry on the first side of the substrate; and

providing the second communication circuitry on the second side of the substrate.

Claim 26 (cancelled).

27. (Original) The method of claim 19, wherein the first and second electrodes are printed on the substrate by a screening process.

28. (Original) The method of claim 19, wherein data is communicated between the first communication circuitry and the second communication circuitry via the capacitive structure.

29. (Previously presented) A computer system, comprising:

a data bus;

a processor coupled to the data bus; and

a modem coupled to the data bus, the modem comprising:

a circuit board having a substrate with a first side and a second side;

a capacitor having a first electrode formed on the first side of the substrate and a second electrode formed on the second side of the substrate; and

a conductive via through the substrate;

system side circuitry coupled to the first electrode, the system side circuitry configurable to communicate with the data bus; and

line side circuitry coupled by the conductive via to the second electrode, the line side circuitry configurable to communicate with a telephone network;

wherein the system side circuitry and the line side circuitry are located on the first side.

30. (Original)The computer system of claim 29, wherein the capacitor provides high voltage isolation between the system side circuitry and the line side circuitry.

31. (Original) The computer system of claim 29, wherein the circuit board is a multi-layer circuit board having a plurality of substrates, the first electrode being formed on more than one substrate.

32. (New) The high voltage isolation barrier structure of claim 1, wherein the circuit board further comprises a substrate having a first substrate and a second substrate, and the capacitive structure comprises:

a first electrode disposed on a first side of the first substrate;

a second electrode disposed on a first side of the second substrate;

a third electrode disposed on a second side of the first substrate and the second substrate, where the first substrate is stacked on top of the second substrate;

a first conductive via through the first substrate, the third electrode, and the second substrate connecting the first electrode and the second electrode and including a high voltage isolation barrier between the first conductive via and the third electrode;

a second conductive via through one of the first substrate or the second substrate connecting to the third electrode; and

wherein the substrate intermediate the first, second and third electrodes functions as a dielectric material within the capacitive structure.

33. (New) The data access arrangement of claim 8, further comprising:

a third electrode contained within the substrate; and

wherein the conductive via through the substrate also extends through the third electrode and includes a high voltage isolation barrier between the via and the third electrode, the first electrode formed on the first side is electrically connected to the second electrode formed on the second side of the substrate, and the capacitor is formed between the first electrode and the second electrode as a first terminal and the third electrode as a second terminal.

34. (New) The method of claim 19, wherein forming the capacitive structure further comprises:

forming a third electrode interior to the substrate;

forming a via through the substrate and the third electrode, wherein the via electrically connects the first and second electrodes and provides a high voltage barrier to the third electrode; and

wherein the substrate intermediate the first, second and third electrodes functions as a dielectric material such that a capacitive structure is formed.

35. The computer system of claim 29, wherein the capacitor comprises:

a third electrode within the substrate;

the first electrode formed on the first side of the substrate and the second electrode formed on the second side of the substrate are electrically connected by the conductive via through the substrate and the third electrode, wherein a high voltage barrier exists between the conductive via and the third electrode.